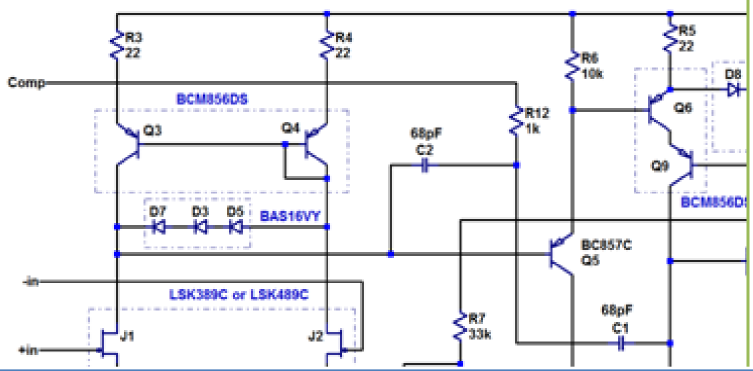


2013

# OPEX-1: a High Performance Class A Opamp for Audio

A low component count Lin topology VFA opamp for audio applications, featuring a matched pair JFET input stage, class A output stage and Two Pole Compensation (TPC). This design features very low distortion: 10V peak into a 600 Ω load is below 1 ppm. The OL UGF is 13 MHz, and the slew rate in excess of 100 V/us. Other than the LSK389C matched JFET pair, the OPEX-1 uses readily available components, and fits on a 6 cm x 4 cm DSTHP PCB. The construction cost for 4-6 pcs is $15 each

Andrew C. Russell

9/1/2013

# OPEX-1: a High Performance Discrete Opamp for Audio Applications.

Sometime around 2009 or 2010, I took an LM4562 and biased into class A, then added a discrete class A buffer stage inside the global feedback loop to produce a high performance class A buffer– you can read about it here, and look at the distortion results in Fig.1 below. In the write up, I focused on the fact that IC opamps always feature class AB output stages, and we know that when driving a heavy load (so, 600 Ω or so in the context of this discussion), they will transition into class B, and the result will be harmonics both in the output signal, and on the supply rails. My effort allowed me to swing a 600 Ω load 20V pk-pk at about 2ppm at 20 kHz, and at 2 or 3 V pk-pk, distortion was about 1.5~2ppm - this measurement result in actuality limited by the performance of the AP Sys272 which has a distortion floor of -114 dB ref 1V into 600 Ω (See Fig 1). Even into 32 Ω, the buffer distortion was in the low single digit ppm level at 2 V output, which is about 30 dB more than your ears could comfortably tolerate on average sensitivity 32 Ω headphones.

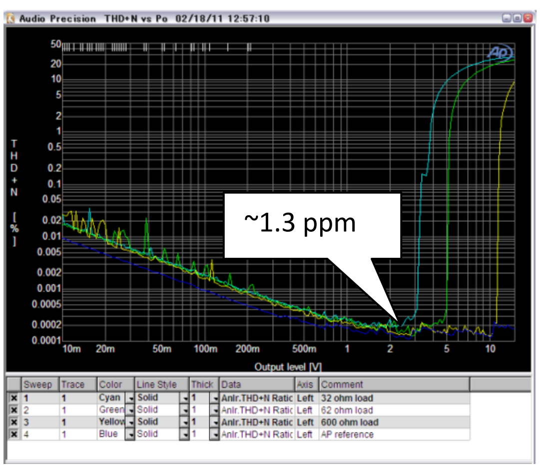


**Figure 1 - The LM4562 Class A Buffer Performance into various loads**

Importantly, all of these performance figures in class A. Now, with good IC opamps the output distortion - even with the transition to class B at low output currents - is still very, very low. The reason for this of course is that the open loop gain is high, and with closed loop gains of 15-20 dB, there is still plenty of loop gain to suppress distortion.

Feedback, or the desire to avoid it, is another hot topic in audio circles. This is a high feedback design: at 10 Hz, the OLG is ~120 dB, while at 100 kHz, it is ~70 dB, with the UGF at 13 MHz. Having designed and built both low high feedback power amplifiers (70 dB feedback at 1 kHz) and low feedback varieties (25 dB at 1kHz) I have concluded that . . . they do sound different, but also sound good. Is feedback the only reason for the difference? No, because between two high feedback designs, or two low feedback ones, there are audible differences, so there are other things in the mix imparting the sonic signature. So, there is no magic formula which says certain levels of feedback, or the absence of it, determine whether an amplifier sounds good or not - the human ear has no preference; instead, it is primed to discriminate on other things like harmonic content (an evolutionary requirement for more clearly being able to identify other individuals in a social group perhaps?). In music, some harmonics sound good, and others quite terrible – so if your design introduces a little bit of $2^{nd}$ or $3^{rd}$ harmonic, it can be very euphonic; $5^{th}$ and $7^{th}$ on the other hand should be avoided. Another area where your ear/brain system excels is in low level sensitivity where it can detect levels down at a few billionths of a watt. Further, there is evidence that human hearing is adept at extracting useful information in the presence of significant levels of uncorrelated noise. I guess these features of our ear/brain system were also the result of evolution, where we were at one stage on some big cats menu, and being able to take evasive action based on information coming in via our ears gave our species a survival edge, however, leaving in our genome the permanent trait of anxiety, if everything we read is to be believed[1].

Leaving evolutionary biology behind, let me add that I have built quite a few opamp based pre-amps and equalizers (and discrete ones as well), so I have *no bias towards either approach*. However, since this is a discrete design, I can address some of the things that IC opamps cannot do particularly well:-

*Class A output stage*. As mentioned above, class B output stages generate distortion and spray signal related harmonics onto the supply lines. With all-class-A operation, you can avoid these drawbacks to a large extent. There is also some strong anecdotal evidence that class A output stages are more euphonic than class AB and class B – my experiences with the sx-Amp certainly seem to support this contention.

*Output Drive Capability*. Modern opamps do a remarkable job of driving quite heavy loads even though operating in class AB – here I am talking about 600 Ω at 10~12 V peak. That old warhorse, the NE5532/34 was one of the first IC opamps designed specifically for audio back in the late 1970's, but its distortion, like that of the modern LM4562, rises at HF into heavy loads. The distortion consists of two types – the class A to class B transition that I mentioned a little earlier on, and a second contributor, the output stage non-linearity due to loading. The action of feedback does a good job of controlling these non-linear mechanisms, but going discrete provides a way to avoid them to a much greater degree.

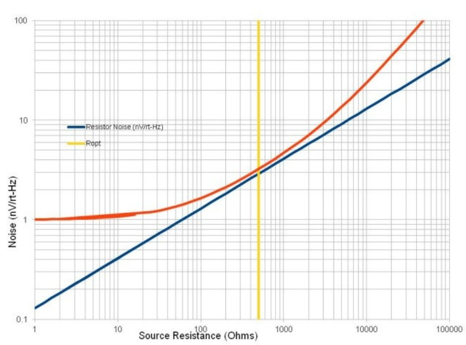


Figure 2 Typical Noise Performance of the LSK389

*Noise*. In terms of input device type, IC opamps come in three flavours: Bipolar, JFET and MOS (which I won't discuss any further here). The best examples of bipolar and JFET types achieve remarkable performance with the AD797 and the LME49990 (2013) the best performers as far as I know for applications being fed from low impedance sources (so, less than 1k Ω), and the AD8xx being a fine example of a JFET input amplifier with good noise performance. There are no IC opamps, at reasonable cost, that I know of that can provide leading edge noise performance across a wide source resistance range. The best bipolar types $e_n$ (equivalent input noise) is considerably lower than JFET types, but their $i_n$ (equivalent

[1] Reminds me of the one about the Neantherdals. Apparently their larger eyes and larger part of the brain associated with vision processing evolved because of the dimly lit northern European winters; this resulted in a reduction in size of the higher reasoning areas of their brains, ultimately leading to their demise. Read about it here and draw your own conclusions . . .

input noise current) is usually substantially higher. If we go discrete, we can select an input device that can offer the potential to cover a much wider input source resistance range with best in class performance. There are two commercially available devices that fit the bill: the Linear Integrated Systems LSK389 at 1nV[2] $e_n$ and 25 pF input capacitance, and their LSK489, with an $e_n$ spec of 1.5nV and an input capacitance of 4pF.

IC opamp designers work within many constraints, and have to make tradeoffs. There is a huge diversity of opamps available on the market, and as pointed out by others in this field, this simply reflects the fact that no single opamp can deliver BIC performance over the full gamut of end applications – and neither can one single discrete opamp either for that matter. One area of course is in power consumption, where a typical IC VFA devices will show Iq figures of less than 10mA. You cannot comfortably dissipate more than a 300mW or so from an 8 pin SOIC package. The discrete designer does not have this constraint, and in the design presented here, the supply current is in the region of 40mA – about half of which is used to bias up the class A output stage.

Of course, in some parameters, IC op-amps absolutely excel, and discrete designers would be hard pressed to beat them in these areas at any level, CMRR being but one example. Input device matching, and the ability to trim resistor values in IA type designs, coupled to the close thermal tracking and small geometries involved (so loop areas are minimal) mean that IC solutions rule. On bipolar input designs, bias currents can be kept very low - for example the LM4562 specifies 10 nA at room temperature, 200nA over the full temp range. No doubt some proprietary fabrication processes, special transistor design, low tail current and innovative compensation techniques, coupled to the fact that the whole circuit is extremely compact, go some way to facilitating this type of performance. Current Feedback Amplifier (CFA) topology designs feature a single active gain stage, and can be configured for very high slew rates (100 ~1000 V/us); these IC designs feature bipolar inputs with high input bias currents in the 2-5 uA range which limits them to low source impedances if you are to avoid coupling capacitors – you cannot feed them directly from a potentiometer because you run the risk of getting 'pot noise'. However, CFA IC opamps excel where speed and settling time are key application requirements. But, if you go discrete VFA, you can elect to run the LTP tail current high, use JFET's for the input pair (preferably monolithic ) and then get high slew rates, and very high input resistance, with the tradeoff being high supply current at 6-7 mA just for the front end, as is the case in the design that will be presented here.

Physical size of course favors IC devices. There are a number of discrete opamps on the market that have the same footprint and pin out as the industry standard 8 pin opamp format. These are usually created using two vertical PCB's, or a single PCB with flying leads to an 8 pin adaptor, which of course means that if care is not taken, they can be susceptible to magnetically and capacitively coupled noise pickup – something monolithic devices are better equipped to deal with. There has been a lot of commentary in various quarters about IC opamps - and

[2] This is the typical figure. Worst case for the LSK389 is quoted at 2 nV

especially bipolar types – susceptibility to RFI, with FET inputs types performing better according to some commentators. I would say that one should never use any amplifier without an input bandwidth limiting filter of some description. If you want to keep effects within the 20 Hz ~ 20 kHz band to 0.1 dB or less, this means the -3 dB cutoff frequency should be set at 200 kHz, which I have found to work very well. Small ferrite beads, through which the signal wire can be threaded at the input connector are also very effective, although some designers say they 'affect the sound'; I can report that I hear no difference. On discrete bipolar opamp designs, you can degenerate the input devices to reduce RFI – but, the penalty is noise – or use a JFET input, where the lower gm provides more protection without the noise penalty, as is the case with JFET input IC opamps.

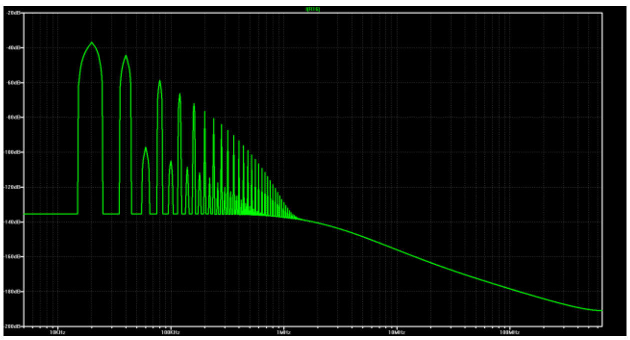
Figure 3 - Class AB Opamp V+ Harmonics

I mentioned a little earlier that one of the reasons to move to an all class A solution was the fact that power supply rail harmonics were substantially reduced. Fig. 4 shows a simulation of an op-amp with the same front end design as the one presented in this document, but with a class AB push pull output – Iq in this case 2.5mA, which is a little better than a typical IC VFA device, but demonstrates my point nonetheless. The distortion at 10 V pk in this design, with TPC, is 2.6 ppm 20 kHz into a 600 Ω load – quit an acceptable number in the company of high performance IC opamps. You can see there is harmonic content in the V+ supply current. With a music signal, the harmonic content would simply be wideband hash up into the hundreds of kHz. Fig 5 shows the same drive and load conditions, but for the class A output stage configuration, where there is less harmonic content, and it is primarily lower order. We know from people like Kendall Castor-Perry[3], that decoupling and layout play a critical role in analog circuit performance and you don't want this type of noise on the supply rails stimulating any resonances in the regulator – decoupling network. A further problem with higher order hash, as per Fig. 4, is that without careful layout, this can couple into the signal path, and this is especially a problem in inverting configurations, where the summing junction is particularly susceptible to capacitively coupled gunk. Armed with these insights, we can now move on to consider the OPEX-1 specifications.

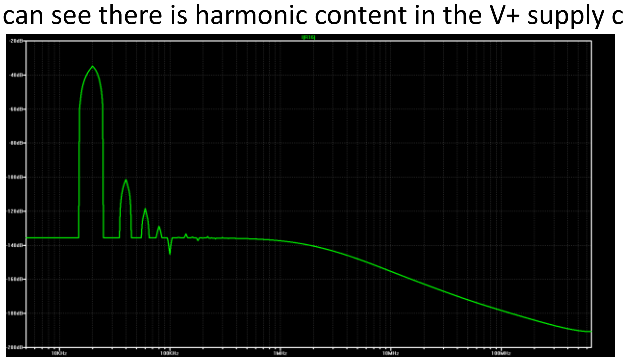
Figure 4 - Class A Opamp V+ Harmonics

[3] See EDN article about PSU and Capacitor interaction

# Specifications

All specifications at 25 ° C and +-17V supply rails unless otherwise noted

| | |
|---|---|
| General Description: | Lin VFA topology, low noise class A Audio operational amplifier |
| Open Loop gain | 120dB at 10 Hz |
| | 70 dB at 100 kHz |
| O.L. Unity Gain Bandwidth | ~ 13 MHz |
| Gain/Phase Margin | >20 dB/>100 degrees (measured at closed loop gain of 16 dB and ULGF of 6 MHz) |
| Slew Rate | >100 V/us |
| Rise/Fall time | 35 ns symmetrical (500 mV step input with Avcl = 16 dB) |
| Compensation | TPC (2 x 68 pF with 1 k to GND) |
| Load Drive Capability | >10 V pk into 600 Ω at 1 ppm distortion at 20 kHz |
| Distortion (non-inverting) | < 1 ppm at 10 V pk into 600 Ω and above up to 50 kHz with Rsource = 150 Ω |
| | ~50 ppb into 600 Ω at 2 V pk at 20 kHz with Rsource = 150 Ω |
| | ~5 ppm into 600 Ω at 2 V pk at 20 kHz with Rsource = 10k Ω |
| | ~30 ppm into 600 Ω at 10 V pk at 20 kHz with Rsource = 10k Ω |
| Input Devices | LSK389 or 2SK389 Low noise dual matched JFET |
| Input bias current | 25 pA typical at room temperature; 10 nA at 125 ° C |
| Input Offset voltage | 5 mV typical; 20 mV max (unity gain) |
| Common mode Rejection | > 70 dB at 1 kHz +ve supply rail; >95 dB on –ve suppy rail |
| Noise Performance | ~ 0.6 uV 20 Hz to 20 kHz (50 Ω source); ~4nV √Hz; Better than -120 dB ref 1 V output with 1 k Ω Source impedance |
| Output stage | Class A into 600 Ω to 10 V peak output |
| PSRR | 70 dB at 1 kHz on positive supply; 100 dB on negative supply |
| Supply Voltage | +-22 V max (requires glue-on heatsink to o/p devices) |
| | +-10 V minimum |
| | +-15 V to +-18 V recommended |
| Power Consumption | <50 mA at +- 22 V |
| Operating Temperature | -20 ° C to +65 ° C |
| DIY Build Cost | approx $20 per unit quantities of 4-6 units – biggest expense being the DSTHP PCB and the LSKx89 dual JFET's |

# Circuit Description and Design Discussion

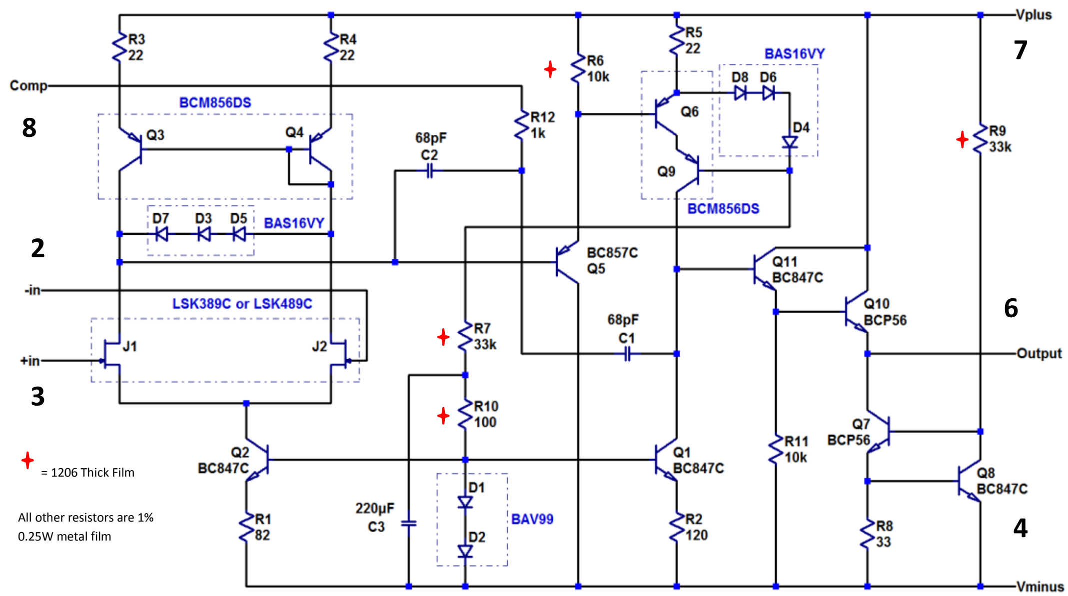


Figure 5 - The OPEX Audio Opamp

The input LTP consists of a dual JFET, LSK389C (for lowest noise) J1 and J2. These feature very low $e_n$ and $i_n$, making this design ideal for amplifying high impedance (so 1 k to 5 k Ω) sources. Q2 is the LTP current source, which in this design delivers ~7.5 mA – this value chosen so that is falls below the LSK389C Idss – which is exceedingly high when compared to IC based opamps; however in this design it gives us the opportunity to build a part with a useful slew rate of 100 V/us. IC designers use other techniques (e.g. current on demand) to achieve this type of performance and low power consumption – we are not constrained by that here. A dual transistor pair, the MCM856DS, forms a current mirror load for the LTP, with the device used here matched and selected in assembly for a Vbe delta between the two transistors of <2 mV, and an hFE match of better than 10%. D3, D5 and D7 provide anti-saturation clamping ensuring the front end comes out of clipping quickly and without any phase reversal, a problem some early IC opamps suffered from.

During the design, I investigated the use of a bootstrapped cascode to the drains of the LTP pair to counteract the problem of gate-drain capacitance which modulates the channel resistance, introducing non-linearity. It was relatively easy to get down to 10 ppb distortion in the simulator at 1.4 V into 600 Ω at 20 kHz (Rsource = 100 Ω). At 10 V output into the same load, but with Rsource set at 10 k Ω, the distortion was about 1.5ppm – both of these measurements good results in my estimation. However, this came at the expense of an additional current source, resistors and the cascode transistors. As I often say, in the interests of practicality, a line has to be drawn in the sand somewhere with regards to complexity. Besides, the PCB real estate in my case is limited.

Q5 provides beta enhancement for TIS stage Q6, which in turn feeds into cascode transistor Q9. On an earlier prototype simulation, leaving this out got 20 k THD best case down to 1ppm at 2 V into 600 Ω, but with the Hawksford technique, this design gets to below 50 ppb – so a 26 dB improvement .

Q1 forms the current source load for the TIS, running at about 7.5mA, just like the LTP current. We could in theory run this at a much lower current, but the negative slew rate would be adversely affected; although they are not symmetrical with the positive slew rate around 218 V/us, I targeted a minimum of 100 V/us, which in this design occurs on the –ve going output slope.

The output stage is a simple current source loaded emitter follower. I could have gone for a diamond buffer or standard complementary output stage biased up into class A, but since the heaviest load is well defined (600 Ω), this approach is effective and provides really excellent performance. For the output stage, I buffered the VAS with a BC847C, driving an 80 V SOT223 BCP56 bipolar transistor. I originally explored the use of a low gate charge mosfet driven directly off the VAS, but eventually settled on the configuration you see here. The gate charge has quite some effect on the fall times, and I could not emulate the 35 ns small signal rise/fall time performance of the two transistor bipolar output stage, although distortion at 20 kHz was also commendably low. Q7, another BCP56, provides the current source load for the buffer and is set at approximately 18 mA in order to support class A operation into 600 Ω at >10V pk. I could have referenced Q7's base to the D1+ D2 diode string, but I did not want the risk of modulating the reference voltage to the LTP and TIS current sources with possible distortion, despite the heavy decoupling by C3 via R10.

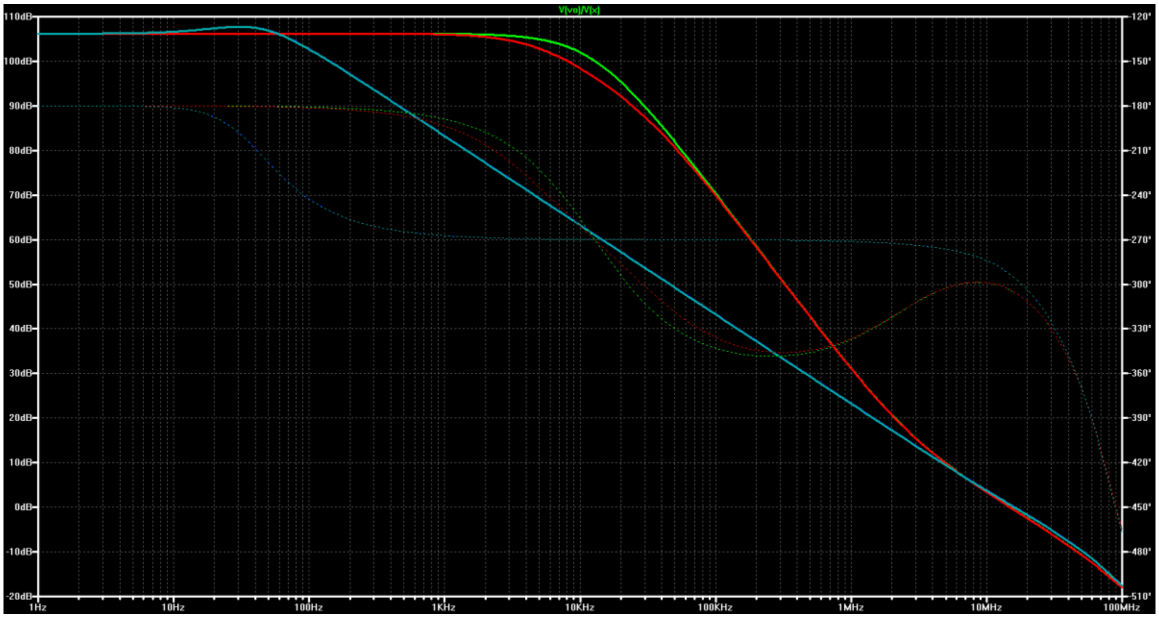

Figure 6 - Loop Gain Response (Acl = 16 dB)

C1, C2 and R12 are arranged to provide Two Pole Compensation (TPC). For classic Lin topology VAF designs, this offers substantial loop gain improvements at HF (so 10 kHz to 100 kHz). Fig. 6 shows the loop gain performance of the scheme with various comp configurations. The blue trace is conventional MC, with Cdom simply the series combination of C1 and C2, yielding 34 pF - accomplished by leaving R12 unconnected (do not ground pin 8). With pin 8 grounded, the loop gain response is the green trace, which provides an additional 35 dB of loop gain at 20 kHz. This translates directly into a circa 50x reduction in distortion at 20 kHz, and is one of the key reasons for the good distortion performance of this opamp at HF. Closed loop gain peaking with TPC can take place, especially if there is significant phase shift in the output stage, but this can be traded for TPC HF loop gain by applying a low value bridge capacitor (3~5 pF given the values of C1 and C2 shown here) across the TPC network (red trace), a technique discussed by Robert Cordell in 'Designing Audio Power Amplifiers', which he refers to as a 'bridged T network'. Given the use of fast output devices, and the recommended 50 Ω output isolation resistor, this is a non-issue in this design. I originally experimented on the simulator with including the output stage in the TPC loop, but ran into stability problems that would have necessitated an additional frequency transition network.

Classic TPC comp schemes usually tie the resistor (R12) to the associated TIS amplifier supply rail, but the penalty is reduced PSRR – whereas the scheme shown in this designe[4] gives about a 30 dB improvement on –ve PSRR at HF. Driving C1 from the emitter of Q11 solves the loop

[4] See Harry Dymond and Phil Mellor's paper here

instability problem I mentioned above, but the fall time is adversely affected, and can only be cured by reducing the value of R11, leading to excessive dissipation. Replacing R11 with a current source would be another option here, but again, we have to consider the added complexity and associated PCB real estate. Again, with distortion sims showing ~50 ppb at 2 V into 600 Ω at 20 kHz, I decided the performance for such a simple circuit was more than adequate.

This opamp, like most of its IC cousins should NOT drive a real world load directly, but through a 50 Ω isolating resistor: If you drive a capacitive load without it, it is likely that oscillations will arise as HF pole migration takes place due to the excess phase shift in the output stage. In this design, the TPC network will provide stability for gains of 2 and above. In a typical line stage, the gain is set to between 14 and 16 dB, which is where this opamp is expected to find application (it will make a fine MM RIAA equalizer opamp as well by the way, with a bit of tweaking to the comp network). Despite the relatively large value of C1 and C2 (68 pF each), this design still manages a respectable slew rate of >100 V/us.

Offset, at unity gain will be 20 mV maximum, with 5 mV a more typical figure. I did not incorporate an offset potentiometer in the LTP sources as in many other designs because I wanted to minimize noise or the requirement for a large bypass cap across the pot, if doing this by adjustment via the input device sources. If you need offset adjustment, this is best done using a 330 k resistor from a 20 k potentiometer connected across the supply rails into the inverting input. Be sure to decouple the offset adjustment resistor well – an example is given in the application circuit a bit later.

As already noted, the PSRR on the rails differ somewhat, with the –ve rail showing a figure of about 30dB higher than the +ve rail. This is a simple single ended design, and the only way to improve the performance is to accept more complexity in the circuit. The easiest way to get the +ve supply rail PSRR to equal that of the –ve rail (so, both around 100 dB at 1 kHz), is to cascode the LTP and then return the compensation capacitor directly to the drain of J1. There is an additional benefit of cascoding, which is that the HF distortion due to Cgd is also reduced – but at 50 ppb already without it, is hardly of any real benefit. I chose to be pragmatic on this point and accept the PSRR differences as you see in the specification – the supply rails are easy to filter, and localized decoupling will go a long way to mitigating this issue, inasmuch as it is a concern at -70 dB on rails that are loaded with fairly constant current demand as is the case here.

Fig 7 shows the rise/fall time performance for 5V pk into a 600 Ω load. The driving signal rise fall times were set to 1 ns for this simulation with no band limiting front end filter. The small signal rise time is ~35 ns.

Importantly, despite the single ended topology, the small signal rise fall times are fairly symmetrical, and this is no doubt attributable to the high TIS stage current which is able, in conjunction with the LTP, is able to sink the tail current on –ve going portions of the waveform.

You should note that with the very fast rise times I used for this test, that there will be overshoot. If more reasonable rise/fall times of 2 us are used, there is no overshoot.

Figure 7 - Stepped Response (500mV input)

Fig 8. Shows the large signal slew response of the opamp, and is confirmed at 218 V/us for the +ve slew rate, and 111 V/us for the –ve slew (not shown – but I have conservatively specified it at >100 V/us ). Since this opamp is designed for small signal applications, this difference in slew rate is of no practical consequence, since it is already very high.

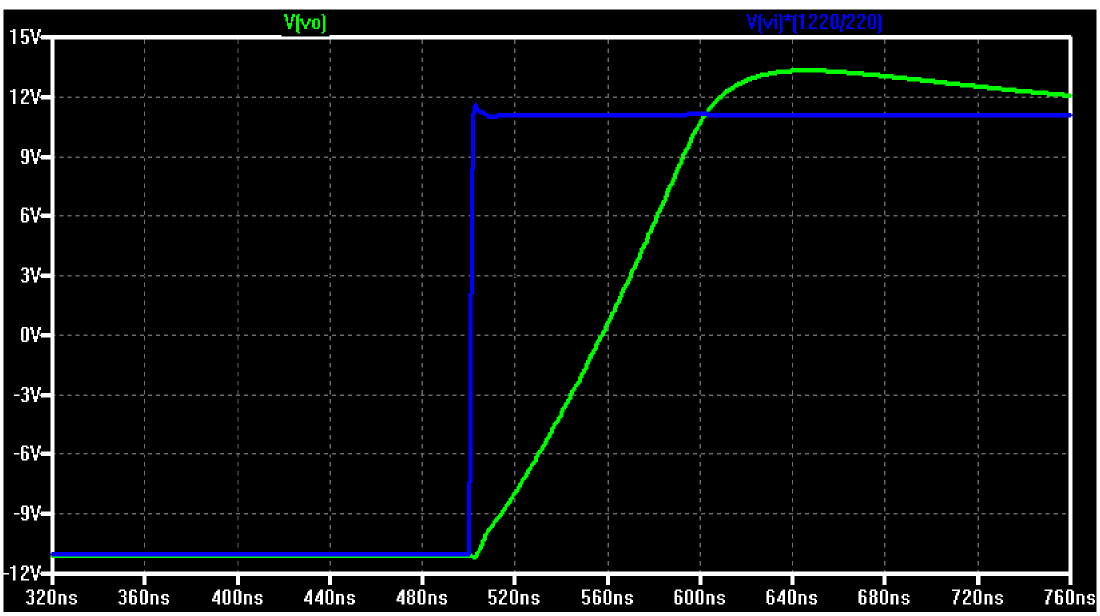


Figure 8 - Large Signal +ve Slew Response is about of 218 V/us, while –ve slew response is well over 100 V/us

# Component Selection and Construction

The resistors marked with a red asterisk in Fig. 3 are 1206 thick film types. Since these are not in the signal path, their non linearity problems will not be manifest. All the remaining resistors must be high quality 0.25W metal film types. I generally like to use Vishay Dale CF types and have found they are very quiet, and have no thermal distortion issues. In an opamp like this that can resolve down to ppb distortion levels, thermal distortion and resistor Voltage coefficient effects are absolutely critical. Especially important are the feedback resistors. The PCB has provision for 2 0.5W MF types for this purpose (yes, these must be mounted on the opamp PCB – I have done this to minimize noise pickup and stray capacitance.). If you mount the resistors off board, the track between the feedback resistors and the –in will be at least 2-3cm's, and that means there is a chance for noise and/or RFI pickup, to say nothing of any parasitic capacitance, which certainly would be an issue if used in an inverting configuration. Doing it as shown, means the connection distance is about 5 mm – a much better situation.

C1 and C2, the compensation capacitors, are good quality polyester film devices, and I do not recommend any other types for this task.

The form factor for this opamp reflects its initial application, which is in my Ovation Symphony preamplifier, while my only concession to convention is the pin out numbering, which follows the usual 8 pin DIP/SOIC industry standard. This means that you can use a standard opamp symbol in a cad drawing, just your package designation would have to reflect the form factor as defined.

# Application Information

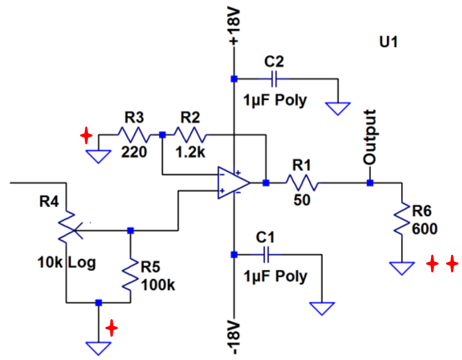


Figure 9 - Standard Application - 16 dB Line Amplifier

Fig 10 shows a typical application circuit. C1 and C2 must be placed close to the supply pins, and must use a short, separate ground return back to the power supply – do not mix this power supply decoupling ground with the signal ground (marked with red *). Similarly, if you can arrange in your circuit to return the output ground (**) back to the power supply, keeping it separate from the * signal ground, you will keep noise and distortion low. Keep in mind, as mentioned earlier, that this opamp is capable of 50ppb distortion performance – the details matter.

You should drive the load through a 47 or 50 Ω resistor (R1) to ensure the opamp is isolated from capacitive load.

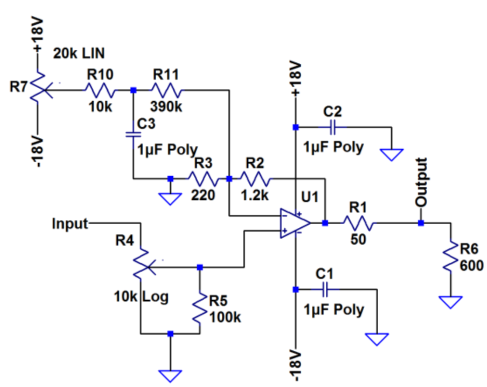


Figure 10 - How to Provide Offset Adjustment

Fig 7 shows how to provide offset adjustment. R11 provides the offset adjust current into the feedback node. You should adjust R7 for 0V output offset with the input signal set to 0V. R10 and C3 provide filtering, to ensure PSU noise is not injected into the feedback node on the opamp –in. Because R11 is in parallel with R3 AC from the AC perspective, its noise contribution is negligible.